REMARKS

Claims 1-30 are present in this application. Claims 8-11 and 21-24 have been withdrawn. Applicants reserve the right to present such claims at a later time in a divisional application. Claims 1, 12, 13, and 14 are independent.

Claim Rejection – 35 U.S.C. § 103; Chan, Sakagami

Claims 1-7, 12-20, 25-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Application Publication 2003/0005214 (Chan) in view of U.S. Patent 5,838,041 (Sakagami). Applicants traverse this rejection.

Claims 1 and 12-14 are directed to embodiments including a semiconductor memory device having a nonvolatile memory section and a volatile memory section, wherein the nonvolatile memory section includes a nonvolatile memory cell having a single gate electrode formed on a semiconductor layer via a gate insulating film, a channel region disposed under the gate electrode, diffusion regions disposed on both sides of the channel region and having a conductive type opposite to that of the channel region, and memory functional units formed on both sides of the gate electrode and having a function for retaining charges.

The Office Action relies on Chan (the '214 reference) for teaching a semiconductor memory device having a nonvolatile memory section and a volatile memory section, and including a logical operation section (claim 12), as well as a portable electronic apparatus having the semiconductor memory device (claims 13 and 14). The Office Action relies on Sakagami (the '041 reference) for teaching specific features of a nonvolatile memory.

The Office Action relies on the first embodiment shown in Fig. 2 of Sakagami to make up for deficiencies in Chan. However, the embodiment shown in Fig. 2 includes diffusion layers 16 and 20 formed as the drain (col. 4, lines 14-15; col. 5, lines 13-18). The charge carrier injection region is provided on the source side (col. 6, lines 48 to 64); the diffusion layer 21 is a source in which an off-set region is provided (col. 4, lines 13-14). Consequently, the first embodiment shown in Fig. 2 is provided with a single memory functional unit that has a function of retaining charges.

In contrast, the nonvolatile memory of the present invention is capable of injecting electrons into both the first memory functional unit and the second memory functional unit, enabling storage of two or more bits.

Thus, Applicants submit that Sakagami fails to make up for deficiencies in Chan as it fails to teach or suggest at least the claimed feature of "memory function units formed on both sides of the gate electrode and having a function for retaining charges," recited in claims 1, 12-14.

Accordingly, Sakagami and Chan, either alone or in combination, fail to teach each and every claimed element of claims 1 and 12-14, as well as respective dependent claims.

Additionally with respect to claim 25, Applicants submit that Sakagami in combination with Chan does not meet the claimed limitation of a volatile memory section having substantially the same structure as the nonvolatile memory section, "except that said volatile memory section has additional extension regions adjacent to the diffusion regions on both sides of the channel region."

To the contrary, Sakagami's nonvolatile memory includes a lightly doped drain region as an additional diffusion region 16 adjacent to diffusion region 20 (Fig. 2).

The Office Action states that Applicants have not disclosed in the specification an advantage for the limitations of claim 25. Applicants submit that an advantage has been disclosed in the specification.

In particular, the present specification does disclose an advantage of having a volatile memory section that has substantially the same structure as the nonvolatile memory section, for example, at the paragraph bridging pages 80-81.

Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection – 35 U.S.C. § 103; Chan, Takahashi

Claims 1-7, 12-20 and 25-30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chan in view of U.S. Patent 6,642,586 (Takahashi). Applicants request that the rejection be withdrawn.

Similar to the above for the rejection based on Chan and Sakagami, Takahashi is relied on for making up for deficiencies in Chan.

The Office Action states that Takahashi teaches in a first embodiment – Fig. 2 – that a nonvolatile memory cell includes charge storage areas (6, 6) on both sides of a single electrode (5) of the cell so as to provide a semiconductor device capable of storing data of two bits in one memory cell and being driven at a low voltage.

Applicants submit that Takahashi also teaches side wall spacers 7 that are electrically connected along with gate electrode 5 to the gate line 10. Further, Takahashi discloses that by electrically connecting the gate electrode 5 to the side wall spacers 7 via the gate line 10, the gate voltage can be applied directly to the side wall spacers 7 in order to lower the gate voltage for write/erase (col. 10, lines 15-19).

Thus, Applicants submit that like Yoshikawa (previously argued), Takahashi teaches a nonvolatile memory that includes side wall spacers 7 serving as electrodes. Therefore, Applicants submit that Takahashi fails to teach or suggest at least the claimed nonvolatile memory cell having a single gate electrode.

Applicants request that the rejection be reconsidered and withdrawn.

Conclusion

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert W. Downs (Reg. No. 48,222) at the telephone number of (703) 205-8000, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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